Design & Hardware Realization of FPGA Based Digital Beam Forming System

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Abstract— **This paper describes the design and in-house development of FPGA based Digital Beam Forming Hardware for 16 elements configuration. Key function of the System involves electronic steering of beam in desired direction to provide anti-jamming feature in communication and navigation satellites. This system has capability to maximize the received power in the direction of signal of interest & minimize the power in the direction of interference. Digital down conversion (DDC) technique is incorporated in the design for providing flexible channel architectures. Dynamic phase calibration and weight uploading facility is included to provide beam forming capability in real time without any hardware penalty.**

Keywords— **FPGA, DBF, DDC, SATCOM**

I. INTRODUCTION

The advances in architecture of satellite communication systems should be capable of preventing exploitation of communication services by intentional jamming from unauthorized user. Anti-jamming techniques are required for a robust communication system free from any interception of communication signals by the jammer. Digital beam forming is an important technique to provide anti jamming feature for any secure satellite system. Secure communication satellites generally use smart antenna technology to provide steerable coverage [1]. This can be achieved using gimballed antennas or array antennas. Array antennas can be used to dynamically place a null in the coverage for blocking the jammer using a technique known as Antenna nulling. Array antennas can also form a peak in the desired direction of received signal to maximize signal of interest. As the total size of the array increases, the central beam width becomes narrower and the side lobes become smaller. So more no. of elements implies greater anti-jamming margin can be provided to the system [2].

Beam forming is the most effective jamming mitigation technique in which antenna radiation pattern of Array antennas can be controlled without physical movement of the antennas. In communications, beam forming is used to point an antenna at the signal source to reduce interference and improve communication quality [3]. In direction finding applications, beam forming can be used to steer an antenna to determine the direction of the signal source. Jamming is the deliberate transmission of radio signals that disrupt communications (navigation) by decreasing the signal to noise ratio of the signal coming from the satellite. Beamforming system is equipped with several antennas and suitable electronics that detect a jamming signal and then point a null in the antenna radiation pattern at the source of the jamming signal.

A digital beam forming algorithm implemented on Actel FPGA which processes digitized input signals received from antenna array elements to determine a set of compensation weights. These input signals are then multiplied by the calibrated weights and summed to output the signal of interest. Digital beam former has flexibility in design and in performance evaluation. The system can be easily manipulated for use in different environments and applications. As an example, we are able to change the weight of the antenna array elements according to any window weighting algorithm to cancel the side lobes. The weight uploading facility incorporated makes the system capable of producing a different number of beams instantly toward different directions based on the number of users, user locations and environmental conditions.

This paper will explain the design and realization of FPGA Based hardware for a digital beam former unit for 16 element configurations which is the most crucial anti-jamming feature for any advanced satellite communication systems. Flexibilities are incorporated in the system for dynamic phase calibration and weight uploading at desired time instant. In addition, channelization is also included in the design to enhance the anti jamming capability of Beamforming system.

This paper is further outlined as follows. Section II discusses the basic architecture of digital beam forming (DBF) system. Section III describes the processing of base band signal in FPGA to place a peak or null in the desired direction. Section IV illustrates the method of dynamic calibration and weight uploading facility incorporated. Section V discusses the hardware realization of DBF system. Section VI concludes the paper and Section VII discusses about the future work followed by acknowledgment.

II. BASIC ARCHITECTURE OF DBF SYSTEM

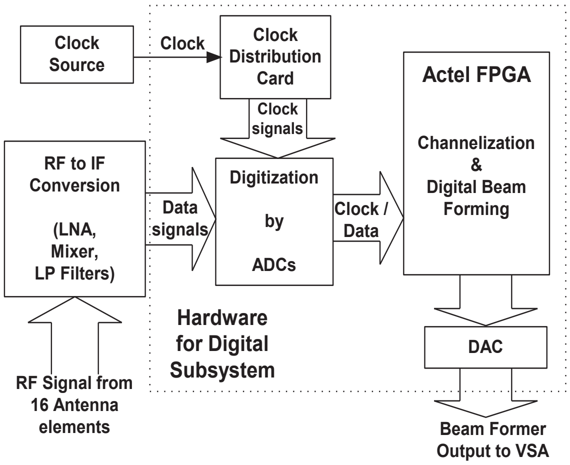

Fig. 1: Basic block diagram of the DBF system

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The block diagram of the 16-element DBF system is shown in Fig. 1. The signal is received using linear array antenna consisting of 16 antenna elements. Each antenna is followed by RF subsystem, which includes LNA, Mixer and Local Oscillators (LO), for down-conversion of received signal to Intermediate Frequency (IF). The IF signal is then filtered and passed to digital subsystem for further baseband processing.

The hardware for digital subsystem consists of the ADCs, Buffers, FPGA and DAC. The most critical requirement for any DBF system is reception of the signals from antenna elements at equal phase for baseband processing. This equi-phase clock distribution is achieved a by a 1:16 clock distribution card which provides equi-phase clock for ADCs for sampling of signals received from 16 numbers of antenna elements. The remaining phase difference is nullified through phase calibration of the digitized signals in calculation of compensation weights. The Actel FPGA used in the digital system consists of main functionalities as channelization followed by digital beam forming operation to provide anti jamming features to the system. The incoming signals from RF subsystem are passed through a set of 16 ADCs and processed in four numbers of Actel FPGAs in the in-house developed digital hardware. Output of the digital system is given to a DAC which is monitored in vector signal analyzer (VSA) to analyze the power in the spectrum which confirms formation of peaks and nulls.

III. FPGA DESIGN FOR PROCESSING OF SIGNAL

The conceptual implementation of DBF system in FPGA is shown in Fig.2. The incoming wideband signal can be split into channels of smaller bandwidth using channelization unit. The different beams at different center frequencies can be generated depending on the interference conditions. The Outputs of individual channels from each respective element is then passed to their respective beam forming systems. This concept is for beam formation for different channels as shown in Fig. 2.

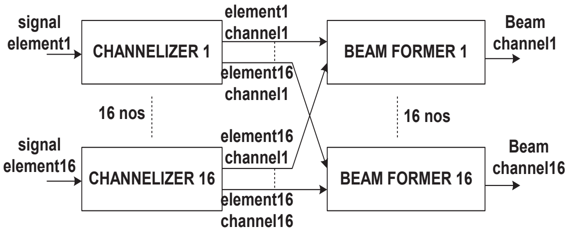

Fig. 2: Concept for beam forming for multiple channels

A. *Digital Down Conversion*

DDC based technique is implemented in this design for channelization. In this technique, the incoming digitized RF wideband signal is shifted from its carrier frequency down to baseband through mixing with a synthesized carrier at or near the carrier frequency of that signal. The resulting signal is then filtered and decimated to extract the channel of interest [5]. The basic block diagram of a typical DDC is given in Fig 3.

The Direct Digital Synthesizer (DDS) is designed to generate the sine and cosine carriers required to mix with the digitized multiplexed input data. The Mixer multiplies the multiplexed input data samples with the synthesized carriers at or near the carrier frequency of the channel of interest to bring the desired channel to the baseband level.

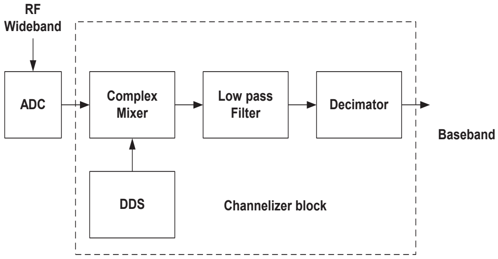

Fig. 3: Basic DDC Architecture

Low pass filtering is required immediately after Mixer to remove the unwanted signal frequencies that would arise due to mixing function and the decimation is essential for reducing the incoming sample rate to the minimum required to relax the signal processing requirements for subsequent stages. Cascaded Integration comb (CIC) filter is used as a low pass filter in the DDC architecture as it is an efficient way of performing decimation along with filtering [6]. These filters are hardware efficient multiplier less filter structures which uses only shifters and adders to perform the filtering function.

B. *Digital Beam Forming Process*

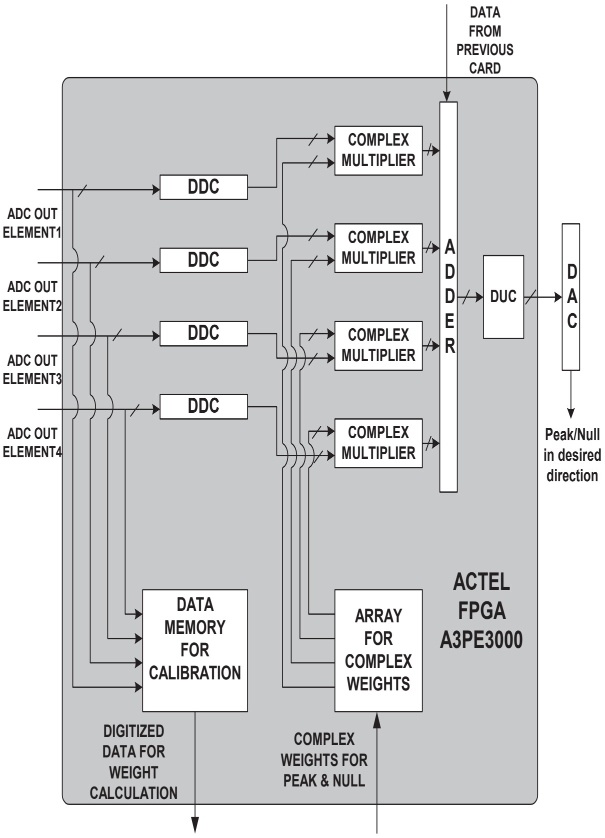

Fig. 4: Block diagram of 4 element DBF System

The complete processing of digitized signal in the FPGA for digital beam forming using 4 elements configuration is shown in Fig. 4. It is further extended by modular approach to accomplish 16 elements configuration. The output of DDC generates baseband IQ signal after down conversion. This baseband signal is multiplied with the set of calibrated weights using complex multiplier and added in proportion to form either a peak or null in the desired direction. The added signal is then translated to the required Intermediate Frequency by using Digital Up- Conversion (DUC) process and passed to DAC. Control logic is implemented for simultaneous capturing of digitized signal for phase calibration and weights computation. Actel ProAsic A3PE3000 is chosen as target FPGA for proof of concept due to its reprogrammability feature and compatibility with antifuse FPGAs available for Actel for flight version [7].

Single digital hardware is designed for four elements configuration which consists of four ADCs, buffers, one Actel ProAsic FPGA and one DAC along with supporting passive elements. Four such identical cards are connected to achieve 16 elements configuration. The flow of data between cards is shown in Fig. 5.

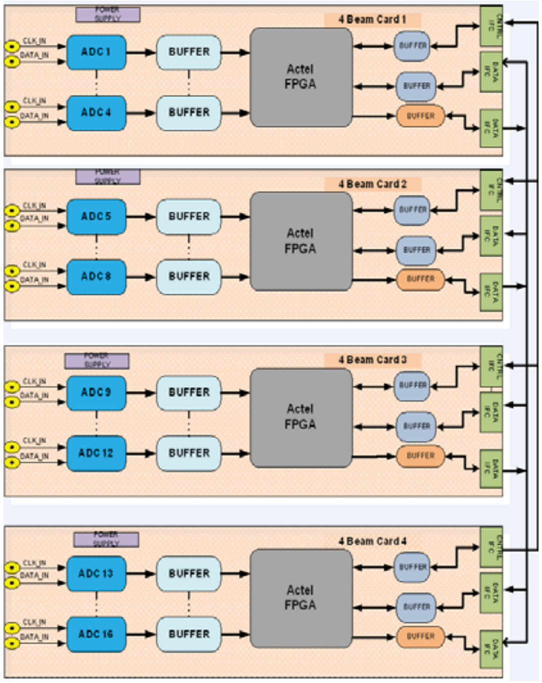

Fig. 5: Data flow for DBF of 16 element configuration

C. *Dynamic Calibration and Weight uploading*

The need of calibration of digitized signals is very important for beam forming as the signals received from various antenna elements are having phase and amplitude imbalance. For maximization or minimization of power at a desired degree it is mandate to do the convolution of signals at same phase or the phase is needed to be cancelled by calibration of the signals for weight calculation [4]. Although the signals are received by identical cables and clock is distributed in equal phase to each ADC, still the difference in phase and amplitude remains due to total RF chain and difference in device related sensitivity.

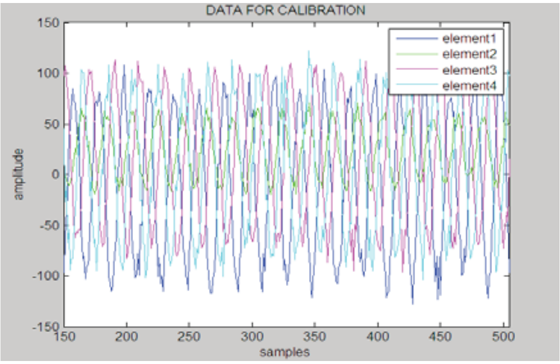

Fig. 6: Digitized data for calibration for 4 elements

Due to this, there is a requirement of dynamic calibration of the signals from all the antenna elements at any instant of time before beam forming operation. So facility is incorporated in the system the system the use of calibration dump blocks for coherent sampling of a chunk of data from each channel on command. This data is then read by PC by RS232 interface and using the Maximum Likelihood approach, sub-sample delay information for amplitude and phase imbalance in each channel is extracted. This information is then converted to compensation weights which are applied along with the nulling weights. 1024 X 8 Block RAMs are used in the Actel FPGA [8] to store 1024 bytes of digitized signal based upon the command given from PC by RS232 interface using MATLAB code. Fig 6 shows the MATLAB plot for sine signal from four ADCs captured in hardware and further given to the PC to be processed in MATLAB for weight calculation. This plot illustrates the difference of phase and amplitude remains in the signal received. This data is processed in MATLAB to generate the weights which are again received in FPGA through same interface and multiplied with the real time signals to form the peak or null at the desired direction.

IV. HARDWARE REALIZATION

The connection between cards is given in Fig. 7. Each card is having three numbers of 25 pin connectors and uni/bi-directional buffers to receive input from previous card and provide output to next card as shown in Fig. 6 and 7. Each card is having facility to observe the output through SMA interface so that modular functionality can be achieved. The SMA output of topmost card is observed in VSA which gives result for 16 elements configuration.

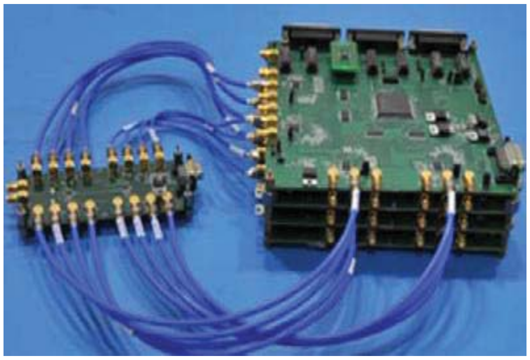

Fig. 7: In-house developed hardware for 16 element configuration

The clock distribution card shown in Fig. 7 generates 16 equi-phase clocks from the single input reference clock which provided to the ADCs so that phase difference in ADCs samples can be minimized and remain constant. The clock to clock skew is in ps at the sampling rate of ADCs so that the relative phase difference between the beams will not get affected by the ADC sampling process. From the output spectrum in loopback test conducted for 8 elements configuration by providing single tone as input signal & giving compensation weights to the system, a null of 27dB is obtained. The gain and phase imbalance caused in cable length and device characteristics in the RF chain are compensated by providing weights generated from calibration algorithm in offline mode.

V. CONCLUSION

A hardware efficient architecture of Actel FPGA based DBF system is presented in this paper for Advanced SATCOM Payload. This POC model has modularity feature since the 16 beam configuration is implemented by 4 identical hardware modules each having 4 element configurations. This gives the advantages of modular functionality verification and flexibility in incremental design and testing. So each unit can verify result for 4 elements and the result for 8, 12 and 16 elements can be observed using the connection of units in required manner. The complete digital hardware is realized using the commercial equivalent of flight model components so that the hardware implementation is compatible for design of flight model.

VI. FUTURE WORK

The design can be modified in to a single card to accommodate 16 elements configuration along with modular functionality. Calibration algorithm for weight generation can be incorporated in the FPGA to make the system more sophisticated.

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